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08/530,661	09/20/95	KEETH B	MI22-356

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HUGH R. KRESS
ARNOLD, WHITE AND DURKEE
P.O. BOX 4433
HOUSTON TX 77210-4433

EXAMINER	
WILLE, D	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 26

Application Number: 08/530,661
Filing Date: 9/20/95
Appellant(s): Keeth et al.

Richard C. Auchterlonie
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed 11/12/99.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's statement that claims 6-10, 18-19, 22-23 and 25-26 stand or fall together is accepted.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

Denboer, A. "Inside Today's Leading Edge Microprocessors" Semiconductor International, Feb. 1994

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 6-8, 18-19, 22-23, and 25-26 are rejected under 35 U.S.C. 112, first paragraph, because the specification does not show how to make devices of the claimed density. The specification describes a technique for fabricating an oxide isolation region which purports to be of a smaller size than standard techniques but provides no teaching of what the degree of improvement might be or how the resultant device compares with other techniques nor is a specific improvement or final size claimed. The specification also shows a method for forming capacitors which purports to increase the effective area using various techniques such as are known in the art but no specific level of improvement is shown or claimed. The specification shows metallization in multiple levels and shows up to four levels while claiming up to five levels but there is no quantitative showing of a specific improvement in device density. Also, although the claims are for a memory cell there is

no showing of any field effect device yet alone CMOS. It would seem that the basic semiconductor device would enter into any method of improving density. Further, the independent claims are for memory devices which have a specified number of devices in an area less than a specified size. For example, claim 6 shows 16 - 17 million memory cells in an area less than 14 mm^2. This also includes an area of say 10 mm^2 or even 1 mm^2 or even less. This then is a claim on all future developments which are part of active research now and also any new techniques that might be developed in the future. In other claims, such as claim 8, the size of a totally unspecified circuitry, which by the way would not benefit for the purported improvements shown in the specification, are claimed. This is totally without basis and can have no enablement in the specification.

If made specific, the specification would enable some level of integration but it is not possible to tell what that level is. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims.

> *"Maximizing density of single transistor and other memory cells is a continuing goal in semiconductor memory fabrication."* (Specification, page 2, lines 7-8)

Between this phrase and applicant's all-encompassing claims, applicant discloses several methods and their resultant structures which applicant claims to produce improved memory cell density. None of these methods, or any of their corresponding structural manifestations, are recited in the

rejected claims. Instead, applicant's claims are written in terms of maximum device density. As such, the scope of applicant's claims includes all devices having the density achieved by applicant as well as all future improvements in density, made through any means, known or unknown. The Federal Circuit has repeatedly held that "the specification must teach those skilled in the art how to make and use the full scope of the claimed invention without 'undue experimentation'." *In re Wright*, 27 USPQ2d 1510, 1513 (Fed. Cir. 1993). With respect to the breadth of a claim relevant to enablement, the dispositive issue is whether the scope of enablement provided to one skilled in the art by the disclosure is commensurate with the scope of the protection sought by the claims. *In re Moore*, 169 USPQ 236, 239 (CCPA 1971).

> "The determination of the propriety of a rejection based upon the scope of a claim relative to the scope of the enablement involves two stages of inquiry. The first is to determine how broad the claim is with respect to the disclosure. The entire claim must be considered. The second inquiry is to determine if one skilled in the art is enabled to make and use the entire scope of the claimed invention without undue experimentation." (MPEP 2164.08)

The scope of applicant's claims includes all semiconductor memory devices of the type claimed, having memory cell density equal to or greater than that achieved by applicant and made through any means at all.

Applicant's acknowledgment of an industry goal to increase the density of memory devices combined with the disclosure's frequent statement that methods other than those

described could be used to form the claimed structure falls far short of enabling one skilled in the art to make the claimed invention through the use of an undisclosed method.

Applicant may be entitled to a patent because no prior artisan has been able to produce the device produced by applicant. However, applicant's claims may not be so broad so as to include within their scope devices which are not enabled by applicant's disclosure. Applicant's disclosure is enabling only for devices made through the use of the disclosed methods and including the disclosed structural features of these methods.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-10, 18-19, 22-23, and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's discussion of the prior art in view of Denboer ("Inside Today's Leading Edge Microprocessors," Semiconductor International, 2/1994).

In applicant's "BACKGROUND OF THE INVENTION," applicant discloses that 16M DRAM chips exist in the prior art (page 2, line 15), that DRAM chips are normally made with

cells arranged in multiple repeating memory arrays, and that "[m]aximizing density of single transistor and other memory cells is a continuing goal in semiconductor memory fabrication." (page 2, lines 7-8) Denboer further discusses the goal of minimizing device size and discusses a structure which achieves a small size and uses 5 conductive layers (note page 2, middle col.) Applicant's claims are written in terms of total combined area of the memory cells or total combined area of the peripheral and pitch circuitry as well as the memory cells. It would have been obvious to one skilled in the art at the time the invention was made to make 16M DRAM chips with ever increasing device density because, as applicant admits, 16M DRAM chips existed in the prior art at the time of invention and because maximizing density of single transistors and other memory cells is a continuing goal in the art. Furthermore, since applicant discloses that one way to achieve the claimed structure is through the use of at least 5 conductive layers and since Denboer teaches the known use of such a structure, the examiner maintains that one skilled in the art would be able to produce the claimed structure.

Applicant's disclosure of the prior art fails to discuss a package having an encapsulating body and electrically conductive interconnect pins extending outwardly from the body, the specific number of cells per array, and the particular number of conductive layers used in the prior art. With respect to the claimed package, such packages are well known to those skilled in the art. With respect to the specific number of cells per array, this number is a function of overall device design and the use of any particular number of cells per array would have been obvious to one skilled in the art at the time of invention depending upon specific device architecture. Finally,

with respect to the number of conductive lines used (a feature which is disclosed by applicant as one which enables production of a structure having the recited density), one skilled in the art would have known at the time the invention was made that semiconductor devices may be fabricated with fewer than, or more than, four conductive layers, as shown by Denboer (figures 1 and 6), depending on particular device design. It would have been obvious to one skilled in the art at the time the invention was made to encapsulate the claimed memory device in a package as recited, to form the arrays with the particular number of cells as claimed, and to include less than four, or more than four, conductive line layers because all these variations are known to those skilled in the art and would have resulted from routine engineering design, optimization, and implementation considerations.

(11) Response to Argument

Applicant's arguments are provided in three sections, A which purports to be a summary of Examiner's rejections but in fact is part of an argument against the rejections, B which is a summary of Applicant's arguments and C which is a discussion of case law as applied to the rejection. Only part B is addressed here.

Applicant here miscategorizes Examiner's argument. What is stated is that while there may be some quantifiable improvement disclosed, it does not enable one to make the invention commensurate with the scope of the claims and this is discussed in detail in the rejection.

Applicant states that a broad claim can be enabled by a single embodiment and should not be rejected because it could read on another embodiment not disclosed or existing. But

note that since the claimed device, in particular claim 6, reads as a claim on a minimum feature size, it is so broad that it would cover any and all inventions that provide a reduced feature size when the are discovered. Since the specification does not disclose features that are not yet invented it is not understood how a valid patent could be obtained on an invention that is not yet made.

Applicant states that the specification contains no language indicating that the claims are to be confined solely to disclosed embodiments (page 7, line 13). Really. Does this mean that the specification can be used to claim anything at all?

Applicant states that it is not necessary to identify every possible way of making a claimed invention but if that is true then he equally cannot claim every possible way of making that invention.

Applicant states that it is improper to limit an apparatus to any particular method. While this is true it is also true that it is proper to limit the apparatus claims to what is enabled by the specification.

Applicant states that the maximum density validly serves to distinguish over the prior art and that is doesn't cover all future improvements since the patent would only be good for 20 years from the date of filing. The period for which the patent would be in force has no bearing on whether enablement is present.

Applicant states that the claims are directed to an apparatus that was admittedly enabling as of the filing date. This is not strictly true, since the specification is enabling of something, but not what was claimed.

Applicant states that Denboer is not enabling for the feature of five conductive layers and hindsight is involved in applying the Denboer article. But Denboer shows the reduction of feature size and the use of the five layer structure. This does not require hindsight, only an understanding of the implied advancement in the state-of-the-art. For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

DAW /k 4c
December 13, 1999

ARNOLD, WHITE & DURKEE
P.O. Box 4433
Houston, Texas 77210-4433